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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/655,321
Filing Date: September 04, 2003
Appellant(s): WATSON ET AL.

Mark E. Scott
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 24 March 2005 appealing from the Office action mailed 22 November 2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect in view of the withdrawn rejection shown below. A correct statement of the status of the claims is as follows:

This appeal involves claims 19, 20, 23, 24, 45, 49, 50, 63 and 65.

Claims 27, 28, 32-34 and 62 are allowed.

Claims 64 and 66 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows: The rejection to claims 27, 28, 32 and 66 under 35 U.S.C. 103 (a) over Kelkar (US Patent No. 5,663,991) in view of Neudeck (US Patent No. 5,701,335) has been withdrawn.

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. The rejection to claims 27, 28, 32 and 66 under 35 U.S.C. 103 (a) over Kelkar (US Patent No. 5,663,991) in view of Neudeck (US Patent No. 5,701,335).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

US Patent No. 5,663,991 to Kelkar et al.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 19, 20, 23, 24, 45, 49, 50, 63 and 65 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelkar et al. (US Patent No. 5,663,991).

With regard to generating first and second reference clock signals, defining a time window and comparing a plurality of cycles of a target clock to the reference clock signals, as shown in claim 19, Kelkar et al. teach defining time slices with references

signals each delayed by a different amount of time and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition on an ASIC (col. 1, lines 13-27; col. 3, line 62 - col. 5, line 2; Fig. 3). With regard to adjusting the time window and repeating the comparing and adjusting to determine the uncertainty window, as shown in claim 19, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions, which would require repeating the comparing and adjusting (col. 6, lines 28-35).

With regard to coupling the core clock to a first and a second adjustable delay chain to created two signals delayed by different amounts, as shown in claim 20, Kelkar et al. teach using different delay on each delay element (col. 3, line 67 - col. 4, line 54; Fig. 2, 3). With regard to defining the time window between corresponding rising edges of the first and second reference signal, as shown in claim 23, Kelkar et al. teach an alternate delay device that uses inverters, which would simply delay the reference clock by a small amount and therefore windows would be between rising edges (col. 5, line 46 - col. 6, line 35; Fig. 5). With regard to adjusting the time window, as shown in claim 24, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions (col. 6, lines 28-35).

With regard to generating four reference clock signals, defining three time bins and comparing a plurality of target clock signals with the reference clock signals, as shown in claim 45, Kelkar et al. teach generating five clock signals that create four time slices and measuring jitter of a clock by determining during which time slice the

transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3). With regard to adjusting the time window and repeating the comparing and adjusting to determine the uncertainty window, as shown in claim 45, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions, which would require repeating the comparing and adjusting (col. 6, lines 28-35).

With regard to defining the time window between corresponding rising edges of the first and second reference signal, as shown in claim 49, Kelkar et al. teach an alternate delay device that uses inverters, which would simply delay the reference clock by a small amount and therefore windows would be between rising edges (col. 5, line 46 - col. 6, line 35; Fig. 5). With regard to adjusting the time window, as shown in claim 50, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions (col. 6, lines 28-35).

With regard to comparing a plurality of cycles of a target clock to a first and second reference clock to determine whether the target clock makes state transitions within a time window, as shown in claim 63, Kelkar et al. teach generating five clock signals that create four time slices and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3). With regard to adjusting the phase of the first and second reference clock, wherein the phases are independently controlled, as shown in claim 63, Kelkar et al. teach adjusting the phase of the time slices and delay

elements with controllable delay (col. 6, lines 28-35; col. 5, lines 46-61; Fig. 5m inverters 1-100).

With regard to a clock domain regions of an electronic device and a jitter measurement circuit with a plurality of independently controlled delay elements and a measurement unit for comparing the target clock to a plurality of reference clock signals, as shown in claim 65, Kelkar et al. teach generating five clock signals that create four time slices and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3).

(10) Response to Argument

Appellant states that Kelkar's adjustment to the delay line is only to ensure that the total delay is maintained equal to one period of the test clock and therefore the bins defined remain constant in spite of process variations, difference in temperature and differences in supply voltage and thus Kelkar fails to teach or suggest "adjusting the phase relationship of at least one of the reference clock signals, and thereby adjusting the time width of at least one time bin." Appellant states that Kelkar teaches away from adjusting the phase relationship to adjust at least one time bin. As pointed out above, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions (col. 6, lines 28-35). While this adjustment is part of a calibration operation the time slices are adjusted and since the time slices are controlled relative to a test clock, a change in the delay is a change in

the phase of the time slices (col. 5, line 62 - col. 6, line 27). Kelkar et al. does not teach away from adjusting the phase relationship to adjust at least one time bin.

In the Final Office Action dated November 22, 2004, the position was taken that "Adjustments of the time windows may be triggered by a change in the frequency of the test clock, or by process variations." Appellant states that they fail to see how Kelkar could teach or suggest "adjusting the phase relationship ... and thereby adjusting the time width of at least one time bin" by "process variations" on a microprocessor die that is already constructed. However, Kelkar et al. teach measuring the error of a phase locked loop on an Advanced Instruction Set Integrated Circuit (ASIC) (col. 1, lines 13-27). Kelkar et al. teach adjusting the time slices for changes caused by process variations and environmental differences (col. 6, lines 28-35). Appellant further states that changing the frequency of the test clock would render the system unable to meet Appellants' claimed measurement of the uncertainty window. While changing the frequency of the test clock would not be reasonable in this situation, the time slices are adjusted to compensate for process variations as shown above.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

mlb

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